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09/880,090	06/14/2001	Yasunori Satoh	OKI 276	3818

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EXAMINER	
NATNAEL, PAULOS M	

ART UNIT	PAPER NUMBER
2614	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/880,090	SATOH, YASUNORI	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims **8-9** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 8 and 9, the claimed phrase "wherein the repetition processing or the deletion processing in the address generation circuit is executed to a rear part of the line of the input data", is not clear where exactly is the rear part of the line of the input data, thus rendering the claims indefinite.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **1-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hickman, U.S. Pat. No. **5,694,432** in view Wang, U.S. Pat. No. **5,796,796.**

Considering claim **1**, Hickman discloses the following claimed subject matter, note;

b) a counter circuit that counts a pixel number of each line in the input data, is met by t FiFo count 48, Fig.4;

c) a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates a new delay in accordance with the delay set by the delay circuit and the delay on the basis of the calculated difference, is met by the Control circuit 53 and multiplexer 44, fig.4.

d) wherein the delay circuit delays the input signal by the delay selected
Is on the basis of the delay calculated by the judgment circuit, is met by the Dual Port Fifo 42;

Except for;

a) a delay circuit that receives the input data, and delays the input data to thereby output as plural output signals, wherein a delay of the delay circuit is selectively variable;

Regarding a), Hickman discloses a Dual Port FIFO 42. Hickman teaches that as another modification, the continuous input series of data bits S.sub.i which occurs on input terminal 10a of the transmitter 10 consists of pixels in successive video frames. These pixels are generated by a camera 160, a sample and hold circuit 161, and an analog-to-digital converter 162 which are serially intercoupled to each other as shown in FIG. 13. (col. 21, lines 10-16) Hickman does not specifically disclose delay circuit

that output as plural output signals. Using multiple delay elements, however, is well known in the art.

In that regard, Wang discloses a pointer adjustment jitter cancellation processor utilizing phase hopping and phase leaking techniques. Fig.3 of Wang discloses the phase hopping controller comprising an array of delay elements 180, an address generator/counter 160, and a multiplexer 170 that selects among the multiple outputs of the delay elements. (col. 5, lines 48-57)

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the reference of Hickman by providing the controller 150 of Wang in order for the system to be able to select from the multiple delayed output signals.

Considering claim **2**, wherein the delay circuit includes plurality of flip-flop circuits, and the plural flip-flop circuits convert the pixels constituting the input data into plural output data with each delayed by one clock,

See rejection of claim 1(a);

Considering claim **3**, a video signal control circuit as claimed in Claim 2, wherein the judgment circuit possesses a selector that selects, on the basis of the calculated delay, a corresponding data out of the plural output data from the delay circuit, is met by Multiplexer 44, fig.4;

Considering claim **4**, a video signal control circuit as claimed in Claim 1, wherein the judgment circuit is able to set an initial value of the delay to the delay circuit in accordance with a selection signal, is met by the DB count 51 and ZD 52, fig.4;

Considering claim **5**, a video signal control circuit as claimed in Claim 4, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial delay in accordance with the inclination of the pixel dispersion.

See rejection of claim 4.

5. Claims **6-7,10-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Urbansky, U.S. Pat. No. 5,859,882.

Considering claim **6**, Urbansky discloses the following claimed subject matter, note; b) an address generation circuit that outputs a write address or a read address to the memory circuit, is met by write counters, 37 and 39, respectively, fig.9;

c) a counter circuit that counts a pixel number of each line in the input data, is met by data analyzer 38, fig.9;

d) a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates a new address value in accordance with an address value generated by the address generation circuit and a delay based on the calculated difference, is met by justification decision circuit 42, fig.9.

e) wherein the address generation circuit generates the write address signal or the read address signal on the basis of the address value calculated by the judgment circuit, and when there is a difference between the pixel number of the input data read from the one-port memory and that of the input data written in the one-port memory, some of the plural read addresses each corresponding to the plural data to be read are repeated or deleted, in accordance with the difference between the pixel numbers, is met by the output of the justification circuit 53, fig.9 which outputs a control signal to the read counter. (col. 9, line 59 through col. 10, line 55)

Except for;

a) a memory circuit which the input data can be written in and read from, which includes two one-port memories, wherein the input data are alternately written in the two one-port memories, and the written input data are alternately read from the two one-port memories;

Urbansky discloses a Buffer 35 (fig. 9). Urbansky does not specifically disclose a two one-port memories. However, Examiner takes official Notice here in that dual port

memories are well known in the art and, therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the reference of Urbansky by providing a dual port memory in order to make the buffer more versatile or useful to the user.

Considering claim **7**, Urbansky discloses the following claimed subject matter, note;
b) an address generation circuit that outputs a write address or a read address to the memory circuit, is met by write counters, 37 and 39, respectively, fig.9;

c) a counter circuit that counts a pixel number of each line in the input data, is met by data analyzer 38, fig.9;

d) a judgment circuit that calculates a difference between a set standard pixel number and the pixel number counted by the counter circuit, and calculates a new address value in accordance with an address value generated by the address generation circuit and a delay on the basis of the calculated difference, is met by justification decision circuit 42, fig.9.

e) wherein the address generation circuit generates the write address signal or the read address signal on the basis of the address value calculated by the judgment circuit, and when there is a difference between the pixel number of the input data read from the memory circuit and that of the input data written in the memory circuit, some of the

plural read addresses each corresponding to the plural data to be read are repeated or deleted, in accordance with the difference between the pixel numbers, is met by the output of the justification circuit 53, fig.9 which outputs a control signal to the read counter. (col. 9, line 59 through col. 10, line 55)

Except for;

a) a memory circuit including a two-port memory that is able to write in and read out the input data in parallel;

Regarding a), see rejection of claim 1(a);

Considering claim **10**, a video signal control circuit as claimed in Claim 6, wherein the judgment circuit is able to set an initial value of the address generated by the address generation circuit in accordance with a selection signal.

See rejection of claim 6 (d) and (e).

Considering claim **11**, a video signal control circuit as claimed in Claim 10, further comprising an initial value judgment circuit that judges an inclination of a is pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial value of the address in accordance with the inclination of the pixel dispersion, is met by the disclosure that "The justification decision circuit 53 produces the control signal SL and at a specific instant receives not only the read clock signal LT, but also an enable pulse FI. If the enable pulse FI occurs, the justification decision is made. The justification decision circuit 53 compares the

value produced by the subtracter 52 via the low-pass filter 61 to a first and a second threshold. The first threshold corresponds to a lower fill of the buffer store 49 and a second threshold to an upper fill of the buffer store 49. If the value produced by the subtracter 52 falls short of the first threshold, negative justification is to be applied, and the control signal SL generated by the justification decision circuit contains an indication about a negative justification action. If the value produced by the subtracter 52 exceeds the second threshold, the control signal SL is produced by the justification decision circuit 53 with a positive justification action." (col. 10, lines 10-25)

Considering claim **12**, a video signal control circuit as claimed in Claim 7, wherein the judgment circuit is able to set an initial value of the address generated by the address generation circuit in accordance with a selection signal.

See rejection of claim 11.

Considering claim **13**, a video signal control circuit as claimed in Claim 12, further comprising an initial value judgment circuit that judges an inclination of a pixel dispersion on the basis of the pixel number counted by the counter circuit, and outputs the selection signal that designates an initial value of the address in accordance with the inclination of the pixel dispersion.

See rejection of claim 11;

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsuchiya et al., U.S. Pat. No. 6,256,003 discloses a jitter correction circuit and a flat panel display device using the same.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 6:30am -3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

MICHAEL H. LEE
PRIMARY EXAMINER

Paulos Natnael PMN
October 8, 2003